THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 38

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte KOJI KINOSHITA

Appeal No. 95-3159
Application No. 08/064,678[1]

HEARD: June 8, 1998

Before THOMAS, HAIRSTON and BARRETT, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1, 3 through 6 and 8 through 12. In a first Amendment After Final (paper number 27), claims 2 and 7 were amended, and, in response to this amendment, the examiner indicated (paper number 28) that claims 2 and 7 were allowed. In a second Amendment After Final (paper number 30), claims 3 and 12 were amended.

[1] Application for patent filed May 21, 1993. According to the appellant, the application is a continuation of Application No. 07/537,303, filed June 13, 1990.

The disclosed invention relates to a multiprocessor system that has a plurality of processors, a main memory common to the plurality of processors, and an access control means coupled between the plurality of processors and the main memory. Each of the processors includes a plurality of vector calculation units. During system execution of a vector calculation, the access control means selectively changes the number of active vector calculation units in each of the processors in accordance with the vector calculation, and the access control means independently enables the active vector calculation units to access the main memory to thereby execute the vector calculation by use of the active calculation units in a pipeline fashion.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A multiprocessor system comprising:

a plurality of processors, each of said processors including a plurality of vector calculation units, each of said vector calculation units executing a vector calculation in a pipeline fashion;

a main memory common to said plurality of processors; and

access control means coupled to said vector calculation units in said processors, respectively, and to said main memory for individually controlling said vector calculation units in each of said processors to selectively change the number of active vector calculation units in each of said processors in accordance with a vector calculation to be executed and to

independently enable said active vector calculation units to access said main memory and to thereby execute a vector calculation by use of said active vector calculation units in the pipeline fashion.

The references relied on by the examiner are:

Hoshino et al. (Hoshino)	4,949,292	Aug. 14, 1990 (Section 102(e) date: Jan. 11, 1989)
Inagami et al. (Inagami)	5,109,499	Apr. 28, 1992 (filed Aug. 29, 1988)

Claims 1, 3 through 6 and 8 through 12 stand rejected under 35 U.S.C. § 103 as being unpatentable over Inagami in view of Hoshino.

Reference is made to the briefs and the answer for the respective positions of the appellant and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection of claims 1, 3 through 6 and 8 through 12.

Inagami is directed to a common vector register 100 (Figures 1 and 2) that is used by a plurality of vector processors 200 through 203 in a vector multiprocessor system. The examiner correctly concluded (Answer, page 3) that Inagami is completely silent concerning a “plurality of vector calculation units” in each of the vector processors. According to the examiner (Answer, page 3), “Hoshino et al. taught a vector processing unit

wherein the processing unit included a plurality of vector calculating units, such as odd term calculating circuit, even term calculating circuit, multiplication circuit, adder circuit...etc. (e.g. see col. 4, lines 6-31)."

Even if we assume for the sake of argument that the plurality of circuits in the vector processing unit of Hoshino are a "plurality of vector calculation units," the claimed limitations of "individually controlling said vector calculation units in each of said processors to selectively change the number of active vector calculation units in each of said processors" (claims 1 and 3 through 5), and "changing the number of the currently active vector calculation units in accordance with said active indication signal" (claims 6 and 8 through 12) can never be met by Hoshino because the plurality of circuits are "simultaneously" operated to solve a recurrent equation (column 6, lines 53 through 55). Stated differently, the number of currently active vector calculation units in Hoshino can never be changed (Brief, page 6). Thus, the obviousness rejection of claims 1, 3 through 6 and 8 through 12 is reversed.

DECISION

The decision of the examiner rejecting claims 1, 3 through 6 and 8 through 12 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)
KENNETH W. HAIRSTON Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
LEE E. BARRETT Administrative Patent Judge	)

Appeal No. 95-3159
Application No. 08/064,678

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Appeal No. 95-3159
Serial No. 08/064,678

1.

Judge HAIRSTON

Judge THOMAS

Judge BARRETT

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Typed: 11 Jun 98

DECISION: REVERSED

Send Reference(s): Yes No

Panel Change: Yes No

3-Person Conf. Yes No

Heard: Yes No

Remanded: Yes No

Index Sheet-2901 Rejection(s): _____

Acts 2: ____

Palm: ____

Mailed:

Updated Monthly Disk: ____

Updated Monthly Report: ___